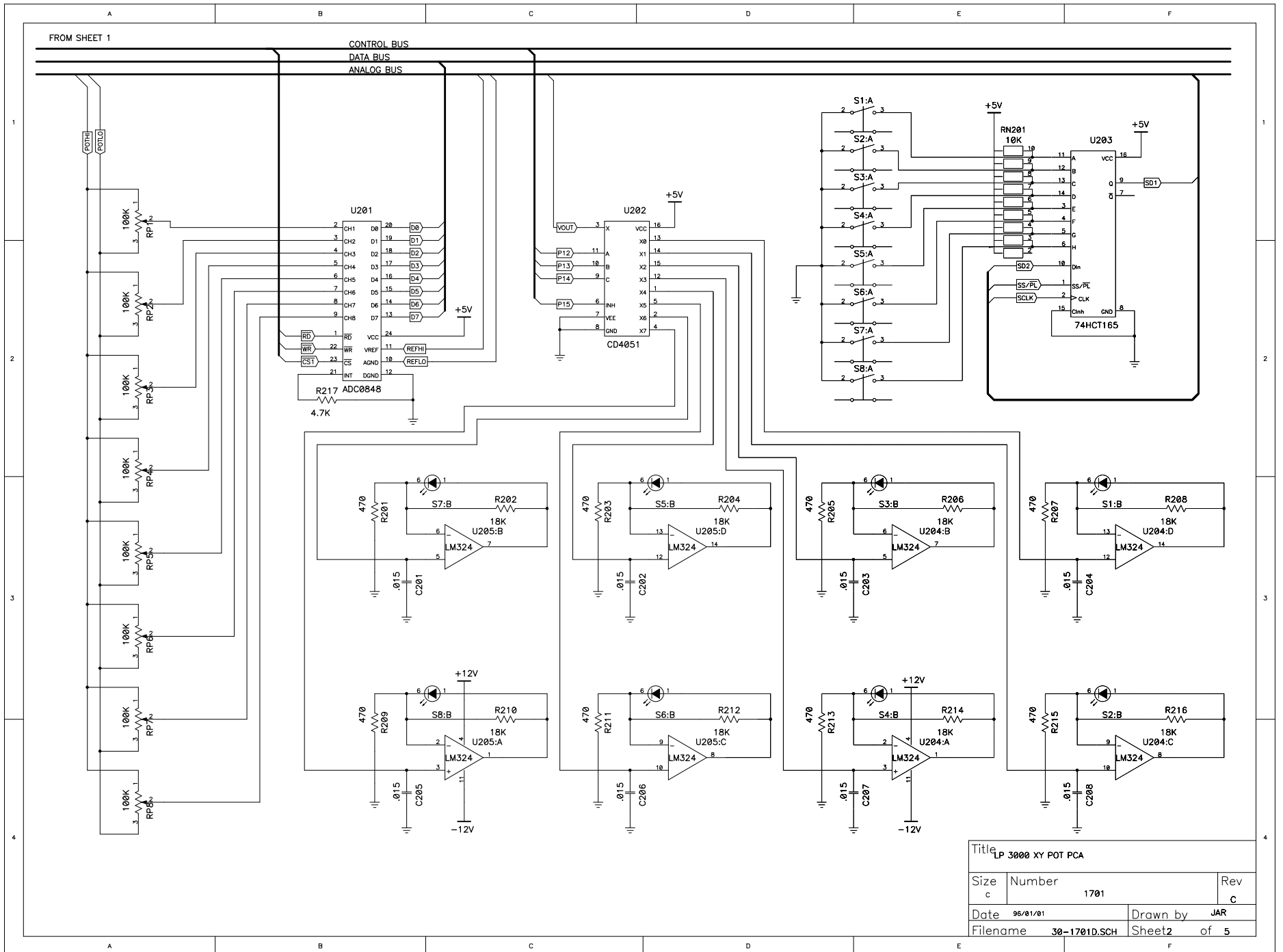


Title			LP 3000 XY POT PCA		
Size	Number	1701		Rev	C
Date	96/01/01		Drawn by JAR		
Filename	30-1701D.SCH		Sheet 1 of 5		

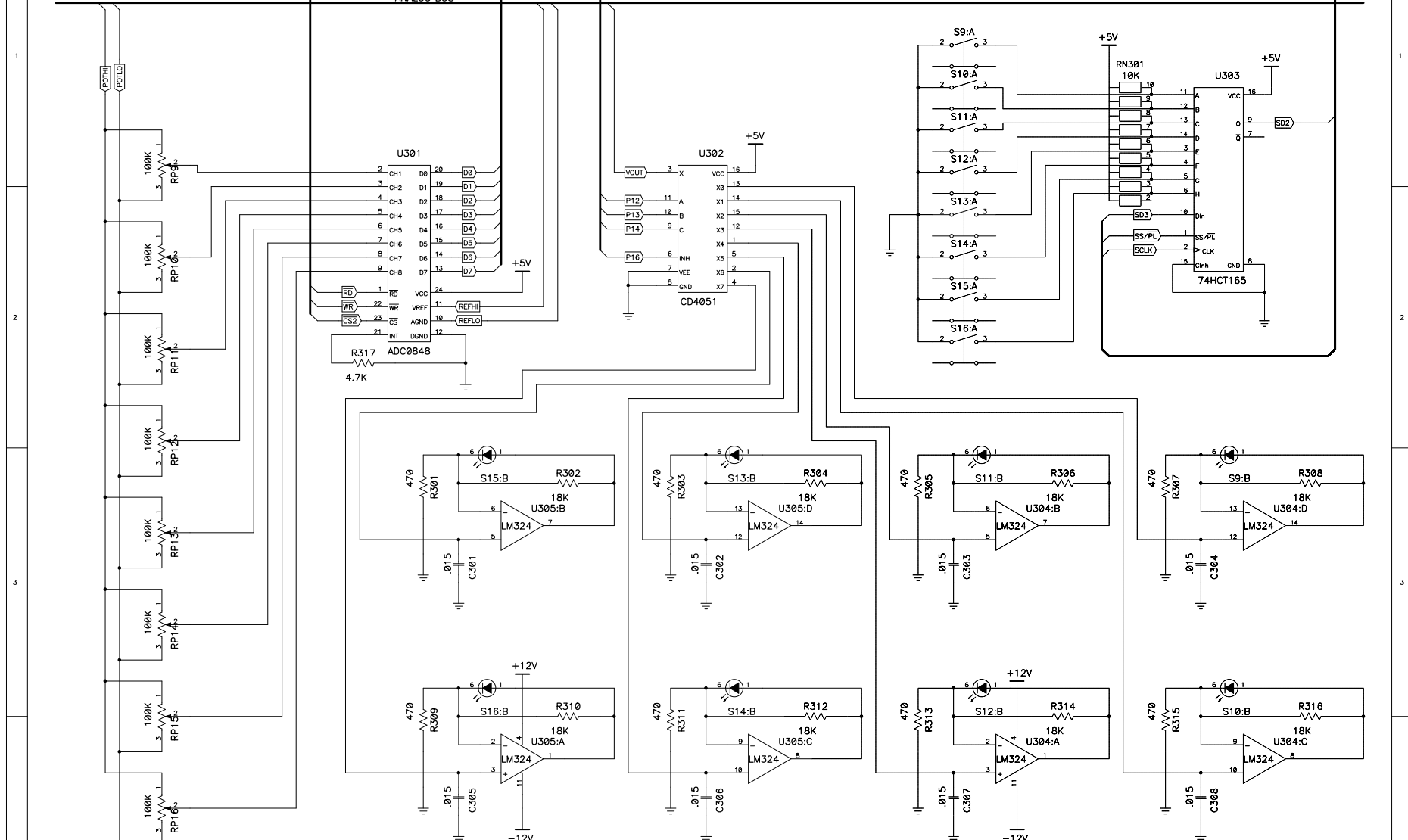


Title LP 3000 XY POT PCA		
Size	Number	Rev
c	1701	C
Date	96/01/01	Drawn by
Filename	30-1701D.SCH	JAR
Sheet of		5

FROM SHEET 2

TO SHEET 4

CONTROL BUS
DATA BUS
ANALOG BUS



Title LP 3000 XY POT PCA		
Size	Number	Rev
c	1701	C
Date	96/01/01	Drawn by JAR
Filename	30-1701D.SCH	Sheet3 of 5

Design notes for layout...

- 1) TP1 is to be placed near center of PCB.
- 2) Connector "TEST1" is a 10 pin, 2 row, 100 mil spacing, 25 mil square post header type.
- 3) One bypass cap.(C103-C126) is to be located near each IC's power pin.
- 4) Analog signal traces are to be separated from digital signal traces.
- 5) POTH1, POTL0, REFH1, and REFLO signal traces are to be 30 mil wide.
- 6) Power and ground traces are to be 50 mil wide.
- 7) A ground plane fill is to be placed under U101.

6/21/95 JAR

Changes and revisions to earlier files for layout...

- 1) J101 and signal traces to it have been changed.
- 2) XR1 and signal traces to it have been changed.
- 3) Testpoints have been reduced to one (see info. above.)
- 4) The file name is changed from 3KXYPOT.sch to 30-1701A.
- 5) A test header has been added (see info above.)

Rev. C Layout Notes

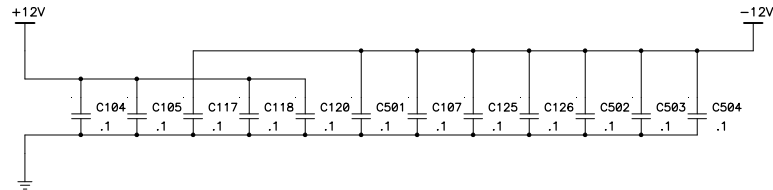
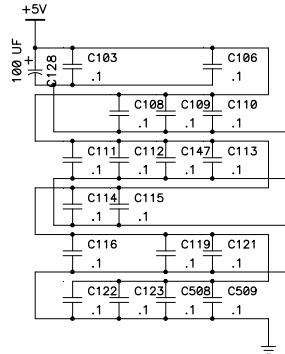
12/14/95 JAR

- 1) Led's 25 and 26 pins are to be corrected.
(flat side is cathode)
- 2) Led's 25 and 26 are to be given a stand-off pin hole.
- 3) Add U108 and U109
- 4) Reconnect J101 Pin 12 to +5V

Rev. D Schematic-only Notes

9/13/96 gaw

- 1) on sheet 1, changed U109 from 6264 to 62256



1701C
1701A
HISTORY

Title		
LP 3000 XY POT PCA		
Size	Number	Rev
c	1701	C
Date	96/01/01	Drawn by
		JAR
Filename	30-1701D.SCH	Sheet 5 of 5