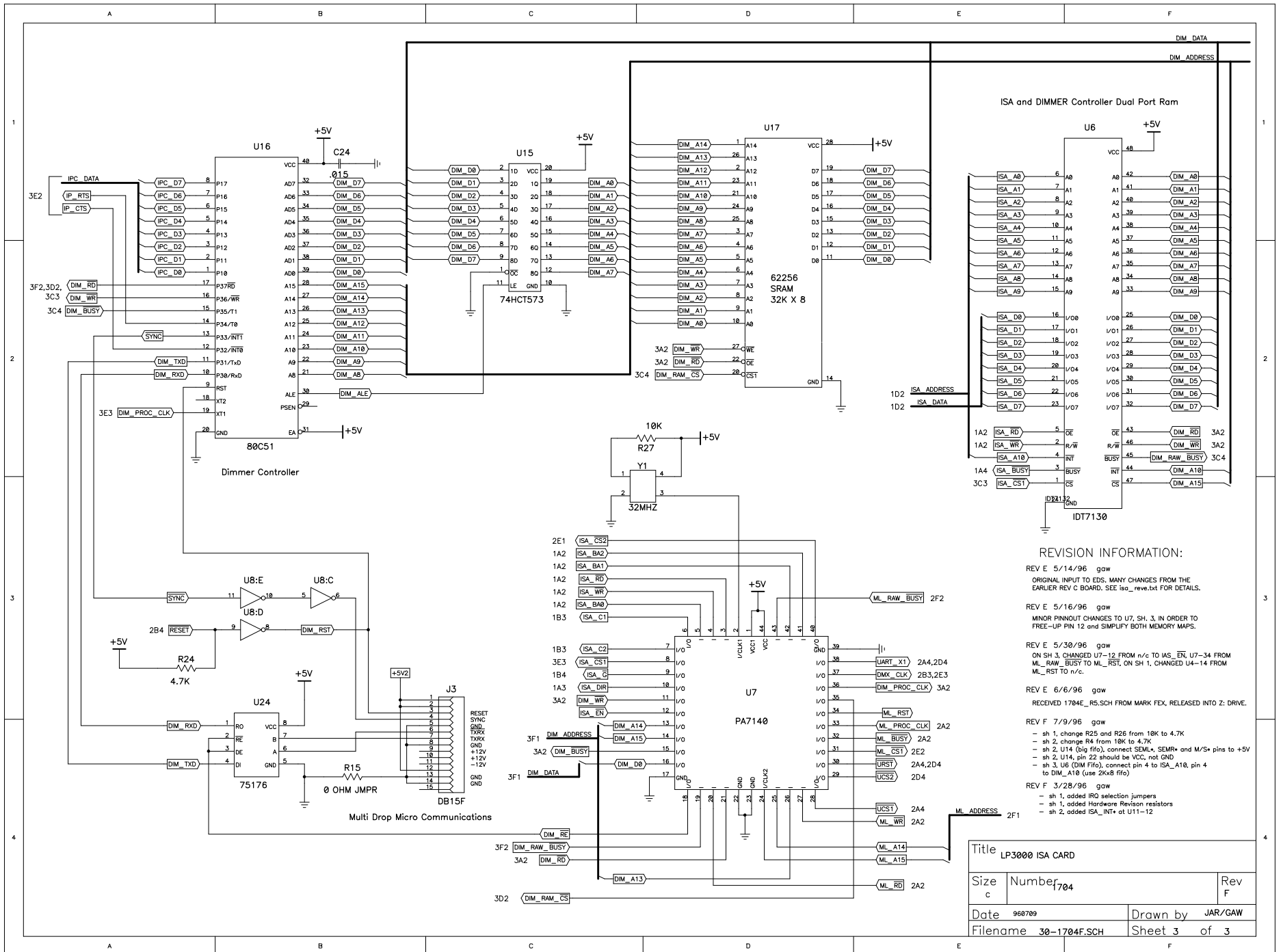


Revision Jumper Chart:

D7	D6	D5	D4	
0	1	1	1	Rev E PCBs
0	1	1	0	Rev F PCBs

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Test points T7 and T8 have been eliminated due to space limitations on PC board.



REVISION INFORMATION:

REV E 5/14/96 gaw
ORIGINAL INPUT TO EDS. MANY CHANGES FROM THE EARLIER REV C BOARD. SEE iso_reve.txt FOR DETAILS.

REV E 5/16/96 gaw
MINOR PINOUT CHANGES TO U7, SH. 3. IN ORDER TO FREE-UP PIN 12 and SIMPLY BOTH MEMORY MAPS.

REV E 5/30/96 gaw
ON SH 3, CHANGED U7-12 FROM n/c TO IAS_EN, U7-34 FROM ML_RAW_BUSY TO ML_RST, ON SH 1, CHANGED U4-14 FROM ML_RST TO n/c.

REV E 6/6/96 gaw
RECEIVED 1704E_RS.SCH FROM MARK FEX, RELEASED INTO 2: DRIVE.

REV F 7/9/96 gaw
- sh 1, change R25 and R26 from 10K to 4.7K
- sh 2, change R4 from 10K to 4.7K
- sh 2, U14 (big fifo), connect SEM+, SEMR+ and M/S+ pins to +5V
- sh 2, U14, pin 22 should be VCC, not GND
- sh 3, U6 (Dim Fifo), connect pin 4 to ISA_A10, pin 4 to DIM_A10 (use 2kx8 fifo)

REV F 3/28/96 gaw
- sh 1, added IRO selection jumpers
- sh 1, added Hardware Revision resistors
- sh 2, added ISA_INT+ at U11-12

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